IN THE CLAIMS

1-27. (Cancelled)

28. (Currently amended) A semiconductor package comprising:

a substrate having a plurality of first printed circuit bond fingers formed on the surface of the substrate;

a semiconductor chip having a plurality of bond pads formed thereon;

a plurality of first printed circuit solder ball pads formed on the surface of the substrate;

a first printed circuit pattern formed on the surface of the substrate ~~between~~ and electrically connecting each of a group of first printed circuit bond fingers and a corresponding first solder ball pad;

a wire bond ~~formed between~~ electrically connecting each of the group of first printed circuit bond fingers and a corresponding bond pad thereby electrically connecting each of the corresponding bond pads to a first solder ball pad;

a second printed circuit bond finger formed on the surface of the substrate;

a second printed circuit solder ball pad formed on the surface of the substrate;

a second printed circuit pattern formed on the surface of the substrate ~~between~~ and electrically connecting the second printed circuit bond finger and the second printed circuit solder ball pad;

a third printed circuit bond finger formed on the surface of the substrate;

a first wire bond having one end affixed to the third bond finger and the other end affixed to one of the bond pads; and

a second wire bond having one end affixed to the second bond finger and the other end affixed to the third bond finger thereby electrically connecting said one bond pad to said second printed circuit solder ball pad.

29. (Currently amended) The semiconductor package of claim 28 wherein there is no printed circuit pattern ~~between~~ directly connected to the third bond finger ~~and any of the solder ball pads~~.

30. (Currently amended) The semiconductor package of claim 29 where there is no wire bond ~~between~~ having one end directly connected to the second bond finger and the other end directly connected to any of the bond pads.

31. (Currently amended) The semiconductor package of claim 28 where there is no wire bond ~~between~~ having one end directly connected to the second bond finger and the other end directly connected to any of the bond pads.

32. (Previously presented) The semiconductor package of claim 28, further comprising:

an encapsulant for encapsulating the semiconductor chip and wire bonds.

33. (Previously presented) The semiconductor package of claim 32, further comprising:

a solder ball connected to said second printed circuit solder ball pad.

34. (Previously presented) The semiconductor package of claim 28, wherein the substrate is a single-layer substrate on which the printed circuit pattern is formed.

35. (Previously presented) The semiconductor package of claim 28, wherein the substrate is a double-layer substrate or a multi-layer substrate.

36. (Previously presented) The semiconductor package of claim 28, wherein a solder mask is not formed on the second bond finger.

37. (Previously presented) The semiconductor package of claim 28, wherein the wire bonds are formed over the substrate.

38. (Currently amended) The semiconductor package of claim 28, wherein the second wire bond ~~between~~ electrically connecting the second bond finger and the third bond finger is formed on an outer region of the substrate on which the semiconductor chip is mounted.

39. (Canceled)

40. (Previously presented) The semiconductor package of claim 28, wherein the semiconductor chip is attached to the substrate using an adhesive.

41. (Canceled)

42. (Currently amended) The semiconductor package of claim 28, wherein the first printed circuit bond fingers have the same pad shape as that of the second bond finger.

43-46. (Canceled)